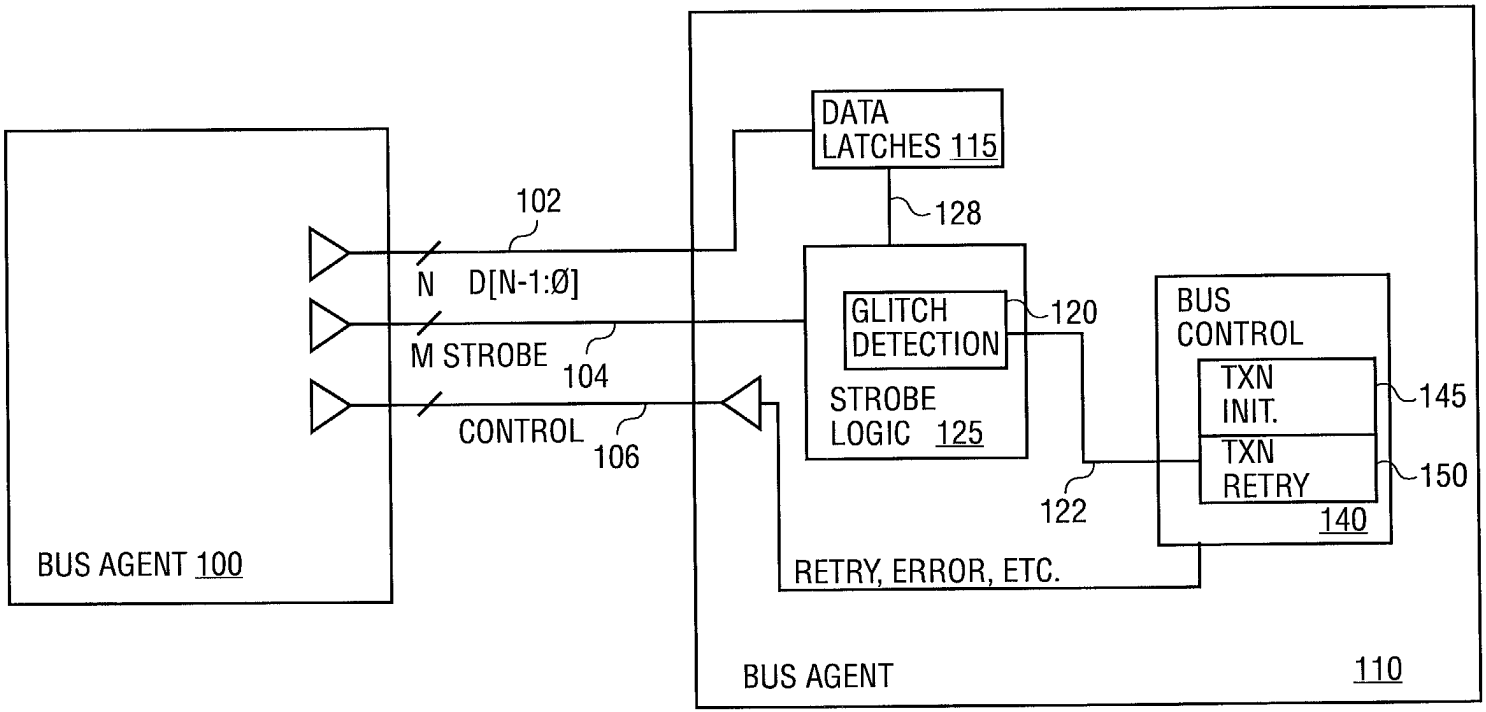

FIG. 1

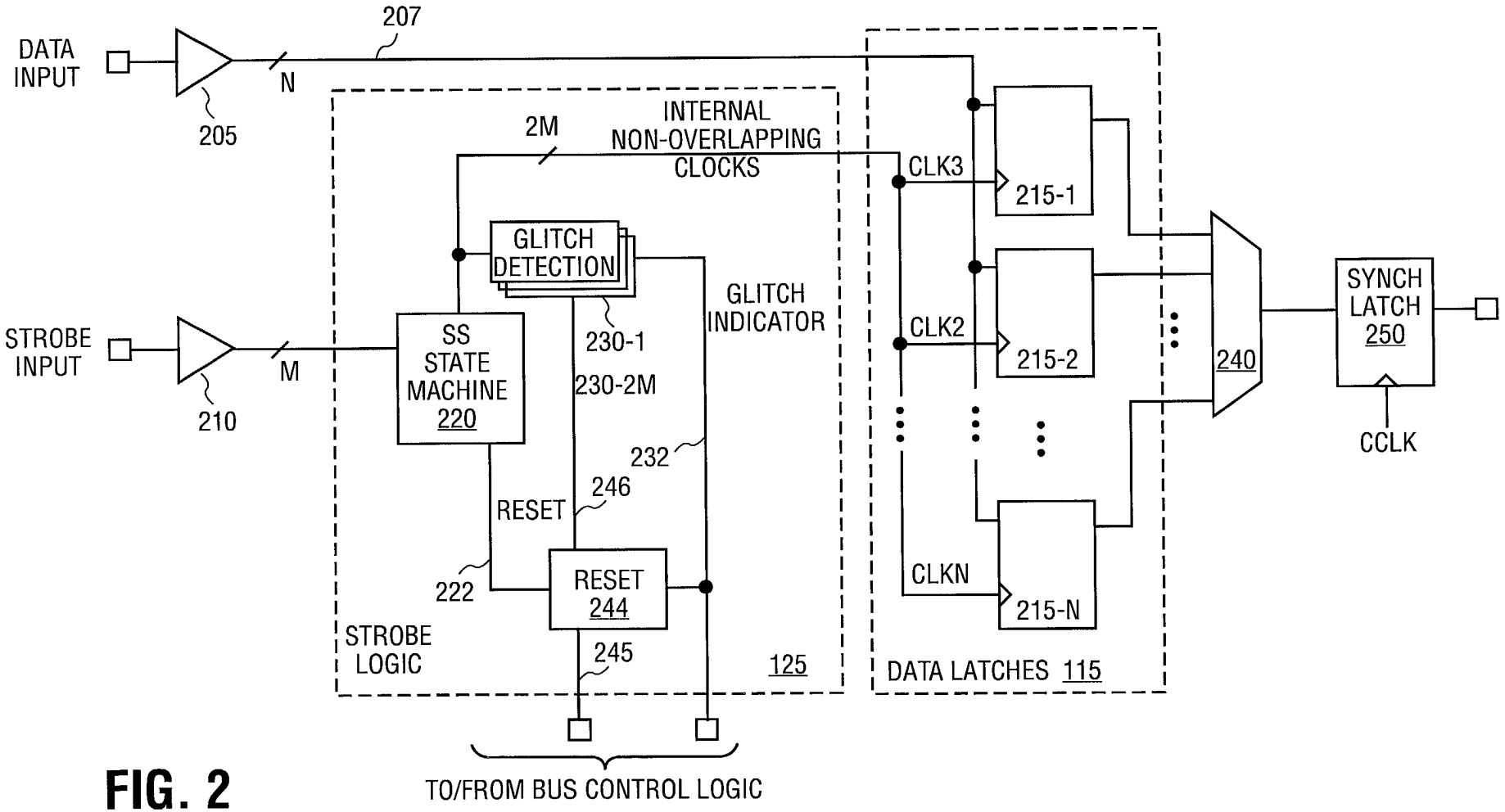
DATA INPUT
205
207
N
2M
INTERNAL NON-OVERLAPPING CLOCKS
CLK3
215-1
GLITCH DETECTION
GLITCH INDICATOR
STROBE INPUT
210
M
SS STATE MACHINE 220
230-1
230-2M
CLK2
215-2
240
SYNCH LATCH 250
CCLK
232
246
RESET
222
RESET 244
CLKN
215-N
STROBE LOGIC
125
245
DATA LATCHES 115
TO/FROM BUS CONTROL LOGIC

FIG. 2

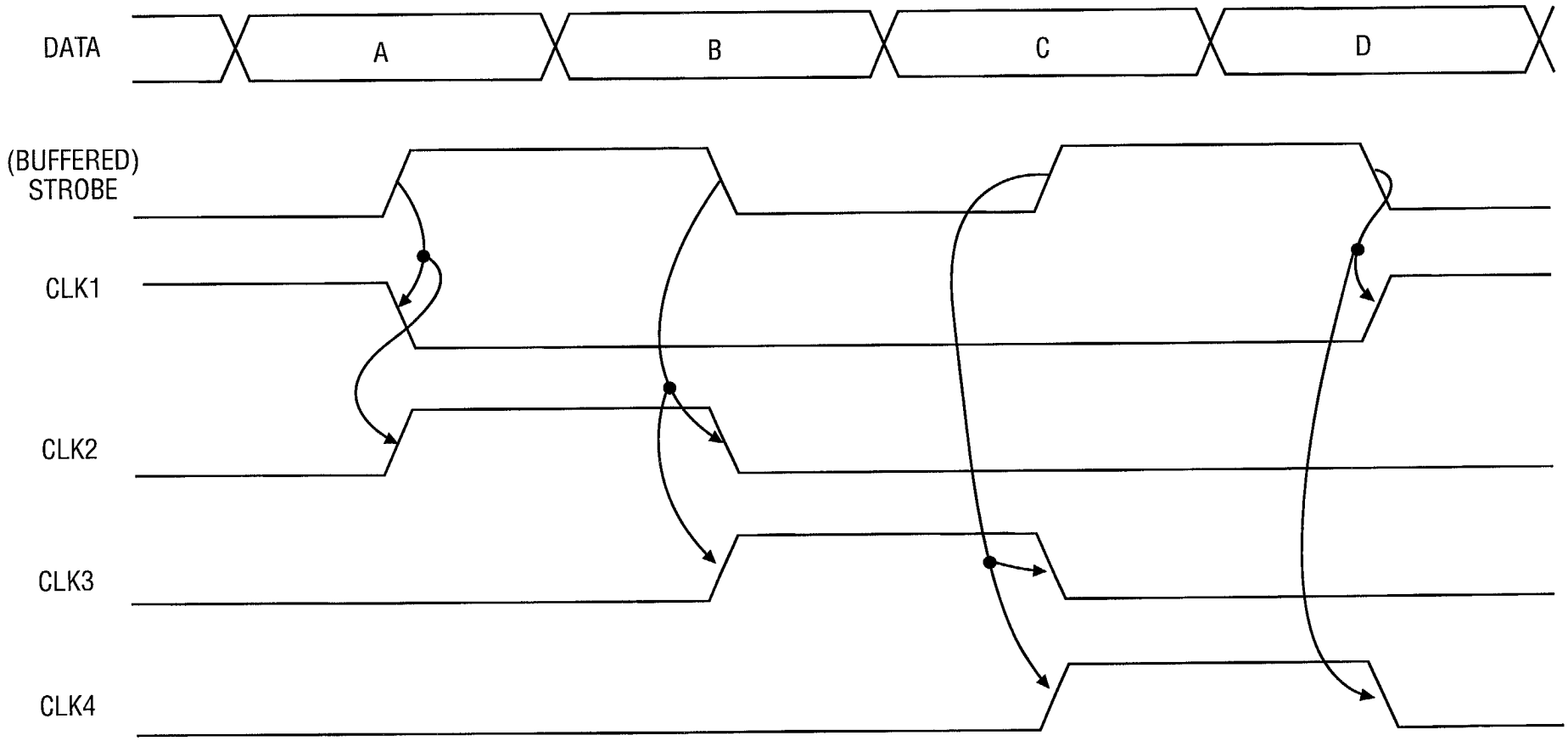

FIG. 3

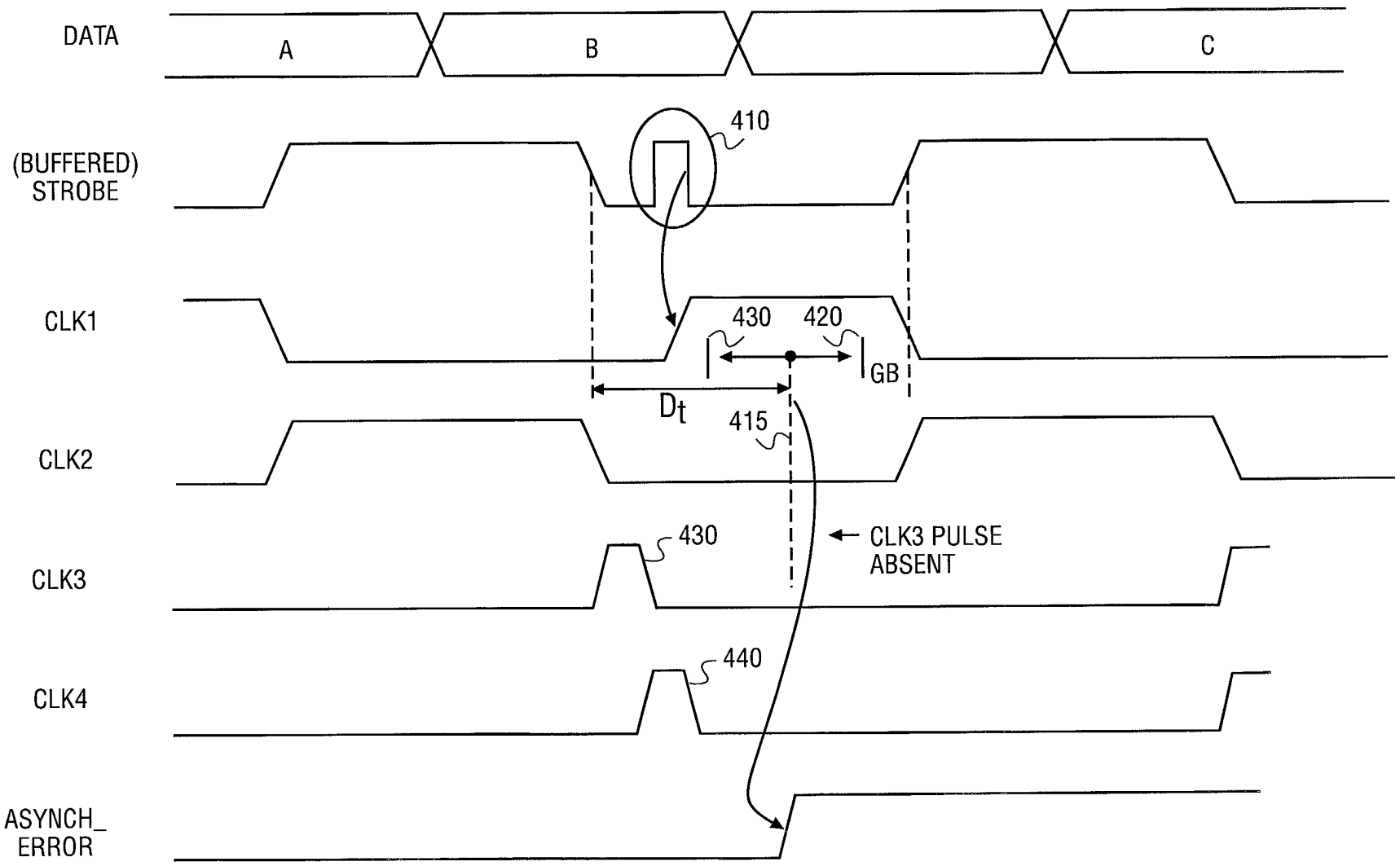
DATA
A
B
C
410
(BUFFERED)
STROBE
CLK1
430
420
GB
Dt
415
CLK2
430
CLK3 PULSE
ABSENT
CLK3
440
CLK4
ASYNCH_
ERROR

FIG. 4

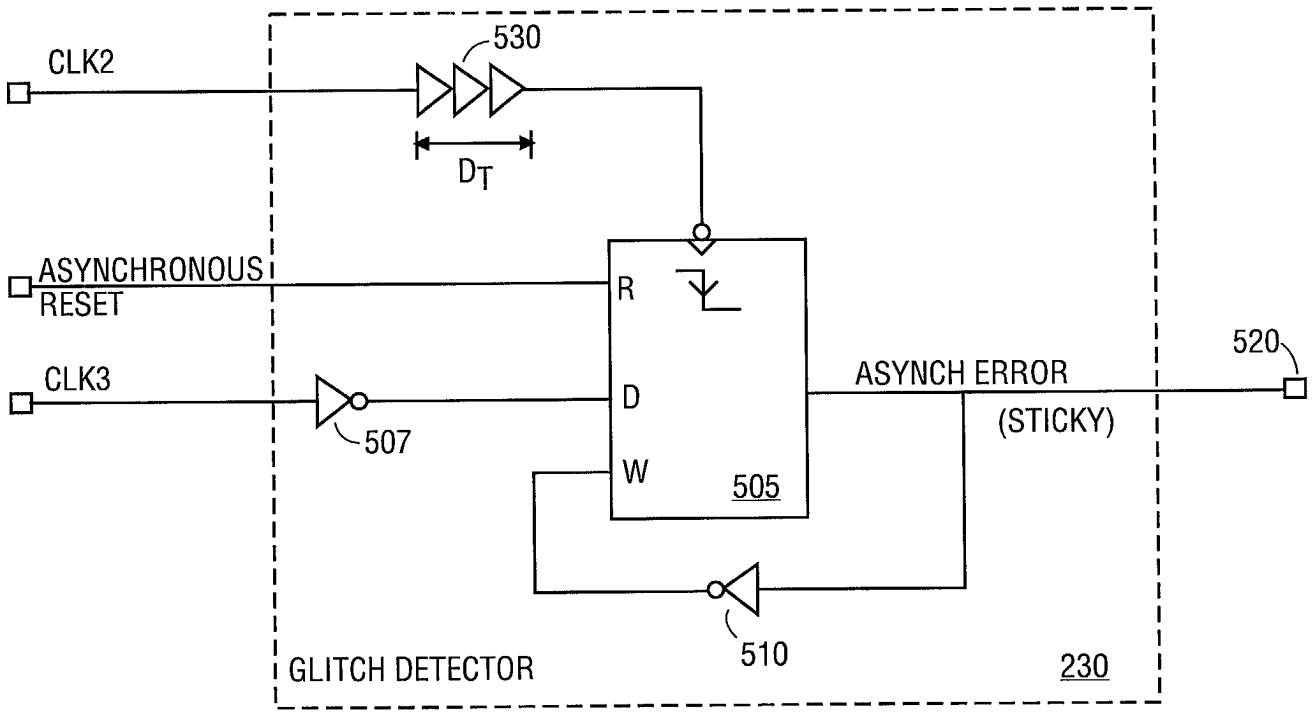

FIG. 5

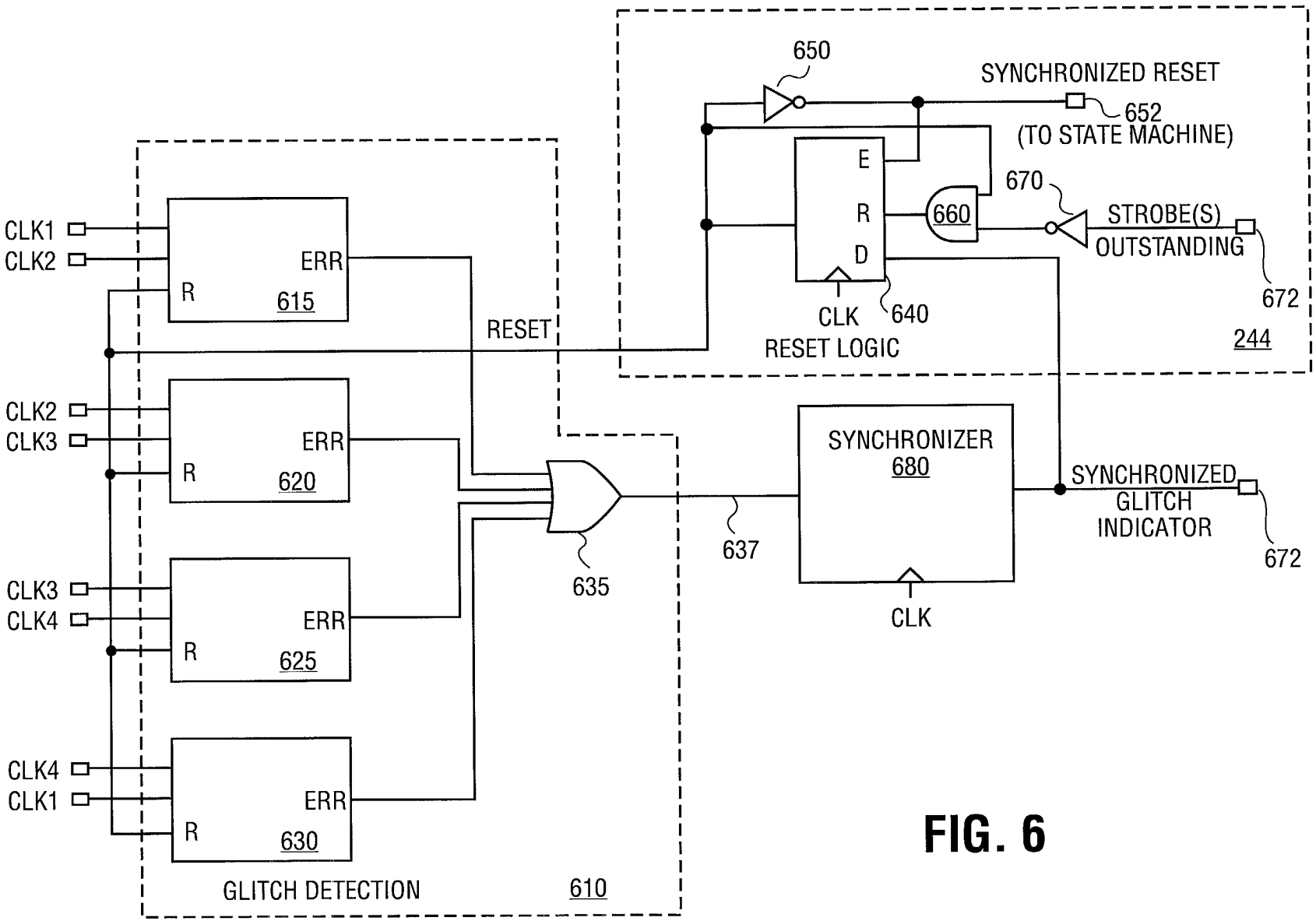
650
SYNCHRONIZED RESET
652
(TO STATE MACHINE)
E
R
D
660
670
STROBE(S)
OUTSTANDING
672
CLK
640
RESET LOGIC
244
CLK1
CLK2
ERR
R
615
RESET
CLK2
CLK3
ERR
R
620
SYNCHRONIZER
680
SYNCHRONIZED
GLITCH
INDICATOR
672
635
637
CLK3
CLK4
ERR
R
625
CLK
CLK4
CLK1
ERR
R
630
GLITCH DETECTION
610

FIG. 6